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EXAMINER	
TRAN, DENISE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/006,785	Applicant(s) MERRITT, TODD A.
	Examiner Denise Tran	Art Unit 2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2002 and 10 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53 and 79-92* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-11,15-19,23-26,30-34,38-43,47-50 and 79-92* is/are rejected.

7)☒ Claim(s) *4-6,12-14,20-22,27-29,35-37,44-46 and 51-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1/30/06* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The applicant's amendment filed 2/9/07 has been considered. Claims 1-53 and new added claims 79-92 are pending in the application. Claims 54-78 have been canceled.

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 79-92 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 54-57 and 60-69 of copending Application No. 10460813. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

4. Claims 1-6 are objected to because of the following informalities: claim 1, line 1, "An output buffers" should be -- An output buffer--. Appropriate correction is required.

5. The indicated allowability of claims 1-53 is withdrawn in view of the newly discovered reference(s) to Park et al., US Patent No. 5,590,086. Rejections based on the newly cited reference(s) follow.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-3, 7-11, 15-19, 23, 31-34, 38-43, and 47-50 are rejected under 35 U.S.C. 102(a) as being anticipated by Park et al., US Patent No. 5,590,086 (hereinafter Park).

Claim 8, Parks teaches an output buffer comprising:

a data mask register including a control terminal adapted to receive a DQM signal, the data mask register generating an output signal a predetermined period after receipt of the DQM signal (e.g., figs. 4 and 31, el. 342; col. 28, lines 1-25);

data output register coupled to the data mask register and including a pair of complimentary data input terminals adapted to receive complimentary data input signals and a pair of data output terminals, the data output register generating respective output signals on the data output terminals having predetermined values responsive to receiving the output signal from the data mask register and having complimentary values corresponding to the data input signals at least part of the time that the output signal from the data mask register is not being received (fig. 26, el. 284, DO and

complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data output terminals of the data output register (e.g., fig. 26, el. 310), the output stage generating a data output signal at an output terminal that corresponds to the output signals from the data output register when the output signals from the data output register do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the output signals from the data output register have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20).

claim I, Parks teaches output buffers, comprising:

a data coder having complimentary data input terminals (fig. 26, DO and complementary DO), a pair of data read output terminals (fig. 26, DO and complementary DO, outputs from 294, 298), and a data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal (fig. 26, el. 284, DO and

complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the data mask register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active (e.g., figs. 4 and 31, el. 342; col. 28, lines 1-25); and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data output register forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder (e.g., fig. 26, el. 310; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20).

Claim 7, Parks teaches an output buffer, comprising:

a data coder having complimentary data input terminals (fig. 26, DO and complementary DO), a pair of data read output terminals (fig. 26, DO and complementary DO, outputs from 294, 298), and a data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder (e.g., fig. 26, el. 310; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage comprising:

a first switch coupled between a first voltage node and the data output terminal (e.g., col. 24, lines 25-35; fig. 26, el. 300, 304, 308 or 306, 302, 308);

a second switch coupled between a second voltage node and the data output terminal (e.g., col. 24, lines 25-35; fig. 26, el. 306, 302, 308 or 300, 304, 308); and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), open the first switch responsive to the one data read signal having other than the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), close the second switch responsive to the other of the data read signals having the second predetermined logic level and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the data output signal has a first logic level responsive to one of the data read output signals having a first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), the data output signal has a second logic level responsive to the other of the data read output signals having a second predetermined logic level (e.g., col. 24, lines 15-35; col. 57, lines 35-65), and the data output terminal has the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels (e.g., col. 37 line 50 to col. 38, line 10), respectively.

Claim 17, Parks teaches a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines (e.g., figs. 1A-1B, fig. 3, A0-A11; col. 6, lines 45-50; col. 7, lines 15-25; 45-50; col. 11, lines 40-55), comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports (e.g., col. 6, lines 45-60; col. 9, lines 35-40);

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array (e.g., col. 10, lines 30-35; col. 13, lines 30-35);

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array (e.g., col.10, lines 35-40); and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array (e.g., col. 22, line 20 o col. 23, line 10), and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-35; fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20) and to

apply the output data signal to the data bit line (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-40), the output buffer comprising:

a data coder having complimentary data input terminals (fig. 26, DO and complementary DO), a pair of data read output terminals (fig. 26, DO and complementary DO, outputs from 294, 298), and a data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the data mask register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active (e.g., figs. 4 and 31, el. 342; col. 28, lines 1-25); and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data output register forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder (e.g., fig. 26, el. 310; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20).

Claim 31, Parks teaches a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines (e.g., figs. 1A-1B, fig. 3, A0-A11; col. 6, lines 45-50; col. 7, lines 15-25; 45-50; col. 11, lines 40-55), comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports (e.g., col. 6, lines 45-60; col. 9, lines 35-40);

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one

of the row lines of the array (e.g., col. 10, lines 30-35; col. 13, lines 30-35);

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array (e.g., col.10, lines 35-40); and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array (e.g., col. 22, line 20 o col. 23, line 10), and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-35; fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20) and to apply the output data signal to the data bit line (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-40), the output buffer comprising:

a data mask register including a control terminal adapted to receive a DQM signal, the data mask register generating an output signal a predetermined period after receipt of the DQM signal (e.g., figs. 4 and 31, el. 342; col. 28, lines 1-25);

data output register coupled to the data mask register and including a pair of complimentary data input terminals adapted to receive complimentary data input signals and a pair of data output terminals, the data output register generating respective output

signals on the data output terminals having predetermined values responsive to receiving the output signal from the data mask register and having complimentary values corresponding to the data input signals at least part of the time that the output signal from the data mask register is not being received (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data output terminals of the data output register (e.g., fig. 26, el. 310), the output stage generating a data output signal at an output terminal that corresponds to the output signals from the data output register when the output signals from the data output register do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the output signals from the data output register have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20).

Claim 23, Parks teaches a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines (e.g., figs. 1A-1B, fig. 3, A0-A11; col. 6, lines 45-50; col. 7, lines 15-25; 45-50; col. 11, lines 40-55), comprising:

an array of memory cells having a plurality of memory coils, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports (e.g., col. 6, lines 45-60; col. 9, lines 35-40);

a row address decoder coupled to the address bus. the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array (e.g., col. 10, lines 30-35; col. 13, lines 30-35);

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array (e.g., col.10, lines 35-40); and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal and to apply the input data signals to respective data ports of the array (e.g., col. 22, line 20 o col. 23, line 10), and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-35; fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20) and to apply the output data signal to the data bit line (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-40), the output buffer comprising:

a data coder having complimentary data input terminals (fig. 26, DO and complementary DO), a pair of data read output terminals (fig. 26, DO and complementary DO, outputs from 294, 298), and a data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines

5-35; col. 37, line 60 to col. 38, line 20), the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder (e.g., fig. 26, el. 310; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage comprising:

a first switch coupled between a first voltage node and the data output terminal (e.g., col. 24, lines 25-35; fig. 26, el. 300, 304, 308 or 306, 302, 308);

a second switch coupled between a second voltage node and the data output terminal (e.g., col. 24, lines 25-35; fig. 26, el. 306, 302, 308 or 300, 304, 308); and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), open the first switch responsive to the one data read signal having other than the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), close the second switch responsive to the other of the data read signals having the second predetermined logic level and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the data output signal has a first logic level responsive to one of the data read output signals having a first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), the data output signal has a second logic level responsive to the other of the data read output signals having a second predetermined logic level (e.g., col. 24, lines 15-35; col. 57, lines 35-65), and the data output terminal has the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels (e.g., col. 37 line 50 to col. 38, line 10), respectively.

Claims 40 and 47, Parks teaches a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines (e.g., figs. 1A-1B, fig. 3, A0-A11; col. 6, lines 45-50; col. 7, lines 15-25; 45-50; col. 11, lines 40-55), comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports

(e.g., col. 6, lines 45-60; col. 9, lines 35-40);

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array (e.g., col. 10, lines 30-35; col. 13, lines 30-35);

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array (e.g., col.10, lines 35-40); and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array (e.g., col. 22, line 20 o col. 23, line 10), and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-35; fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20) and to apply the output data signal to the data bit line (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-40), the output buffer comprising:

a data coder having complimentary data input terminals (fig. 26, DO and complementary DO), a pair of data read output terminals (fig. 26, DO and complementary DO, outputs from 294, 298), and a data mask control terminal (fig. 26,

el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder (e.g., fig. 26, el. 310; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage comprising:

a first switch coupled between a first voltage node and the output data bit (e.g., col. 24, lines 25-35; fig. 26, el. 300, 304, 308 or 306, 302, 308);

a second switch coupled between a second voltage node and the output data bit (e.g., col. 24, lines 25-35; fig. 26, el. 306, 302, 308 or 300, 304, 308); and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65), open the first switch responsive to the one data read signal having other than the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65), close the second switch responsive to the other of the data read signals having the second predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65) and open the second switch responsive to the other data read signal having other than the second predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65).

Claims 2-3, 9-11, 18-19, 32-34, 41-43, 48-50, Parks teaches the predetermined values of the data read output signals are any values in which the data read output signals at the respective first and second data read output terminals have the same value (i.e., OTRST= 0, output of 296, 298 have the same values 1; e.g., col. 24, lines 15-35; col. 28, lines 1-10); the predetermined values of the data read output signal correspond to logic "1" (i.e., OTRST= 0, output of 296, 298 have the same values 1; e.g., col. 24, lines 15-35; col. 28, lines 1-10); wherein the data output register generates the output signals on the respective data output terminals having predetermined values contemporaneously with receiving the output signal from the data mask register (i.e.,

OTRST= 0, output of 296, 298 have the same values 1; e.g., col. 24, lines 15-35; col. 28, lines 1-10; col. 26, lines 10-15); the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the data mask register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active (e.g., figs. 4 and 31, el. 342; col. 28, lines 1-25); and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data output register forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20).

Claims 15-16 and 38-39, Parks teaches the output stage comprises a logic circuit that causes the data output signal to have a first logic level responsive to one of the output signals from the data output register having a first predetermined logic level (e.g., col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65), that causes the data output signal to have a second logic level responsive to the other of the output signals from the data output register having a second predetermined logic level (e.g., col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65), and that cause the data output terminal to have the relative high impedance responsive to both of the output signals from the data output register having other than the first and second

predetermined logic levels (e.g., col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65); the output stage comprises:

a first switch coupled between a first voltage node and the output data bit (e.g., col. 24, lines 25-35; fig. 26, el. 300, 304, 308 or 306, 302, 308);

a second switch coupled between a second voltage node and the output data bit (e.g., col. 24, lines 25-35; fig. 26, el. 306, 302, 308 or 300, 304, 308); and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65), open the first switch responsive to the one data read signal having other than the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65), close the second switch responsive to the other of the data read signals having the second predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65) and open the second switch responsive to the other data read signal having other than the second predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 37, line 60 to col. 38, line 20; col. 57, lines 35-65).

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 24-26 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al., US Patent No. 5,590,086 (hereinafter Park), in view of Mano, Computer System Architecture, 1982, pages 264-265.

Claim 24, Parks teaches a computer system, comprising:

a processor (e.g., col. 1, line 10-15);

an input device coupled to the processor (e.g., abstract):

an output device coupled to the processor (abstract, col. 9, lines 35-45; col. 24, lines 5-10);

a memory controller coupled to the processor (e.g., col. 11, lines 45-50; abstract); and

a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines at least some of which are coupled to the memory controller (e.g., figs. 1A-1B, fig. 3, A0-A11; col. 6, lines 45-50; col. 7, lines 15-25; 45-50; col. 11, lines 40-55), the dynamic random access memory comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports (e.g., col. 6, lines 45-60; col. 9, lines 35-40);

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array (e.g., col. 10, lines 30-35; col. 13, lines 30-35);

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array (e.g., col.10, lines 35-40); and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array (e.g., col. 22, line 20 o col. 23, line 10), and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-35; fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20) and to apply the output data signal to the data bit line (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-40), the output buffer comprising:

a data coder having complimentary data input terminals (fig. 26, DO and complementary DO), a pair of data read output terminals (fig. 26, DO and complementary DO, outputs from 294, 298), and a data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input

terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the data mask register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active (e.g., figs. 4 and 31, el. 342; col. 28, lines 1-25); and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data output register forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder (e.g., fig. 26, el. 310; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output

stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20). Parks does not explicitly show a processor data bus, address bus, and control bus. Mano shows show a processor data bus, address bus, and control bus (e.g., page 265, fig. 7-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Mano into the system of Parks because it would allow communication between the CPU and memory in the system as taught by Mano, page 265, paragraph 3.

Claim 30, Parks teaches a computer system, comprising:

a processor (e.g., col. 1, line 10-15);

an input device coupled to the processor (e.g., abstract):

an output device coupled to the processor (abstract, col. 9, lines 35-45; col. 24, lines 5-10);

a memory controller coupled to the processor (e.g., col. 11, lines 45-50; abstract); and

a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines at least some of which are coupled to the memory controller (e.g., figs. 1A-1B, fig. 3, A0-A11; col. 6, lines 45-50; col. 7, lines 15-25; 45-50; col. 11, lines 40-55), the dynamic random access memory comprising:

an array of memory cells having a plurality of memory coils, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports (e.g., col. 6, lines 45-60; col. 9, lines 35-40);

a row address decoder coupled to the address bus. the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array (e.g., col. 10, lines 30-35; col. 13, lines 30-35);

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array (e.g., col.10, lines 35-40); and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal and to apply the input data signals to respective data ports of the array (e.g., col. 22, line 20 o col. 23, line 10), and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-35; fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20) and to apply the output data signal to the data bit line (e.g., fig. 23, DO, complementary DO, el, 284; col. 24, lines 5-40), the output buffer comprising:

a data coder having complimentary data input terminals (fig. 26, DO and complementary DO), a pair of data read output terminals (fig. 26, DO and complementary DO, outputs from 294, 298), and a data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal (fig. 26, el. 284, DO and complementary DO, outputs from 294, 298; fig. 31, DQM; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20); and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder (e.g., fig. 26, el. 310; col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values (e.g., col. 24, lines 5-35; col. 37, line 60 to col. 38, line 20), the output stage comprising:

a first switch coupled between a first voltage node and the data output terminal (e.g., col. 24, lines 25-35; fig. 26, el. 300, 304, 308 or 306, 302, 308);

a second switch coupled between a second voltage node and the data output terminal (e.g., col. 24, lines 25-35; fig. 26, el. 306, 302, 308 or 300, 304, 308); and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), open the first switch responsive to the one data read signal having other than the first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), close the second switch responsive to the other of the data read signals having the second predetermined logic level and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the data output signal has a first logic level responsive to one of the data read output signals having a first predetermined logic level (e.g., fig. 26, el. 310, OTRST; col. 24, lines 15-35; col. 57, lines 35-65), the data output signal has a second logic level responsive to the other of the data read output signals having a second predetermined logic level (e.g., col. 24, lines 15-35; col. 57, lines 35-65), and the data output terminal has the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels (e.g., col. 37 line 50 to col. 38, line 10), respectively. Parks does not explicitly show a processor data bus, address bus, and control bus. Mano shows show a processor data bus, address bus, and control bus (e.g., page 265, fig. 7-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made

to apply the teaching of Mano into the system of Parks because it would allow communication between the CPU and memory in the system as taught by Mano, page 265, paragraph 3.

Claims 25-26, Parks teaches the predetermined values of the data read output signals are any values in which the data read output signals at the respective first and second data read output terminals have the same value (i.e., OTRST= 0, output of 296, 298 have the same values 1; e.g., col. 24, lines 15-35; col. 28, lines 1-10); the predetermined values of the data read output signal correspond to logic "1" (i.e., OTRST= 0, output of 296, 298 have the same values 1; e.g., col. 24, lines 15-35; col. 28, lines 1-10).

10. Claims 79-92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al., US Patent No. 5,590,086 (hereinafter Park).

As per claim 83, Park shows a method of selectively masking complimentary read data signals responsive to a data mask signal (e.g., figs. 26, 31-32, 54), comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and a second clock edge of the clock signal (e.g., col. 28, lines 1-25);

generating first and second coded read data signals corresponding to the complimentary read data signals, respectively, in the absence of the data mask signal

(e.g., figs. 26, DO, complementary DO, 288, 290, outputs from 294, 298; col. 37, line 35 to col. 38 line 20);

a predetermined period after receipt of the data mask signal (e.g., figs. 26, 53, DO, complement DO, els. 288, 290, outputs from els. 294, 298; col. 37, line 35 to col. 38 line 20), coding the first and second coded read data signals in a predetermined manner responsive to the data mask signal (e.g., figs. 26, 53, DO, complementary DO, els. 288, 290, outputs from els. 294, 298; col. 37, line 35 to col. 38 line 20);

generating on a data output terminal an output signal having a value determined by the first and second coded read data signals if the coded read data signals are not coded in the predetermined manner (e.g., figs. 26, 54, el. 308, DQ; col. 37, line 35 to col. 38 line 20), the output signal being generated by coupling the data output terminal to a first voltage if the first coded read data signal has a first value, and coupling the data output terminal to a second voltage if the second coded read data signal has the first value (e.g., figs. 26, 54, el. 308, DQ, els. Vcc, Vss, Vpp; col. 37, line 35 to col. 38 line 20); and

placing the data output terminal at a high impedance by isolating the data output terminal from the first and second voltages if the coded read data signals are coded in the predetermined manner (e.g., figs. 26, 54, el. 308, DQ; col. 37, line 35 to col. 38, line 20) . Parks does not explicitly shows a second latency setting; however, Parks teaches the time adjustment may be accomplished by changing the number of the shift stages (i.e., a second latency setting) (e.g., col. 28, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to register a signal

representing the data mask signal in response to a second clock edge of the clock signal for a second latency setting by changing the number of the shift stages (i.e., second latency setting) because it would allow time adjustment of inhibiting data output and increase system flexibility and performance as taught by Parks, (e.g., col. 28, lines 20-25; col. 3, lines 1-5).

As per claim 79, Park teaches a method of masking data coupled through a data output buffer responsive to a data mask signal applied to the output buffer (e.g., figs. 26, 31-32, 54), the output buffer having first and second stages connected in series with each other (e.g., fig. 26, els. 286, 286'and 300, 304, 306), the method comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and a second clock edge of the clock signal (e.g., col. 28, lines 1-25);

coupling the first and the second input terminals at which complimentary first and second data signals are applied, respectively, to respective first and second output terminals of the first stage when the data mask signal is inactive (e.g., fig. 26, DO, complementary DO, 288, 290; col. 37, line 35 to col. 38 line 20);

generating a control signal responsive to a predetermined portion of a clock signal after the data mask signal become active (e.g., figs. 26, 31, Clk, YEP, DQMS, TRST; col. 37, line 35 to col. 38 line 20),

Applying respective predetermined signals to the first and second output terminals of the first stage responsive to the control signal (e.g., figs. 26, 53, DO, complementary DO, els. 288, 290, TRST; col. 37, line 35 to col. 38 line 20);

Applying a data output signal to an output terminal of the second stage corresponding to the complimentary first and second data signals when the respective predetermined signals are not being applied to the first and second input terminals of the second stage (e.g., figs. 26, 54, el. 308, DQ, outputs from 294 and 298; col. 37, line 35 to col. 38 line 20); and

tri-stating the output terminal of the second stage when the respective predetermined signals are being applied to the first and second input terminals of the second stage (e.g., figs. 26, 54, el. 308, DQ, outputs from 294 and 298; col. 37, line 35 to col. 38 line 20). Parks does not explicitly shows a second latency setting; however, Parks teaches the time adjustment may be accomplished by changing the number of the shift stages (i.e., a second latency setting) (e.g., col. 28, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to register a signal representing the data mask signal in response to a second clock edge of the clock signal for a second latency setting by changing the number of the shift stages (i.e., second latency setting) because it would allow time adjustment of inhibiting data output and increase system flexibility and performance as taught by Parks, (e.g., col. 28, lines 20-25; col. 3, lines 1-5).

As per claim 85, Park teaches a method of masking data coupled through a data output buffer responsive to a data mask signal applied to the output buffer (e.g., figs. 26, 31-32, 54), the output buffer having first and second stages connected in series with each other (e.g., fig. 26, els. 286, 286'and 300, 304, 306), the method comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and a second clock edge of the clock signal (e.g., col. 28, lines 1-25);

coupling the first and the second input terminals at which complimentary first and second data signals are applied, respectively, to respective first and second output terminals of the first stage when the data mask signal is inactive (e.g., fig. 26, DO, complementary DO, 288, 290; col. 37, line 35 to col. 38 line 20);

Applying respective predetermined signals to the first and second output terminals of the first stage responsive to the control signal, respectively, to the second stage when the data mask signal is active (e.g., figs. 26, 53, DO, complementary DO, els. 288, 290, TRST; col. 37, line 35 to col. 38 line 20);

Coupling an output terminal of the second stage to a first voltage node responsive to one of the data read output signals having a first predetermined logic level (e.g., figs. 26, 54, el. 308, DQ, els. Vcc, Vss, Vpp; col. 37, line 35 to col. 38 line 20);

Coupling the output terminal of the second stage to a second voltage node responsive to the other of the data read output signals having a second predetermined logic level (e.g., figs. 26, 54, el. 308, DQ, els. Vcc, Vss, Vpp; col. 37, line 35 to col. 38 line 20); and

Electrically isolating the output terminal of the second stage from the first and second voltage nodes responsive to both the data read output signals having other than the first or second predetermined logic levels (e.g., figs. 26, 54, el. 308, DQ; col. 37, line 35 to col. 38 line 20). Parks does not explicitly shows a second latency setting; however, Parks teaches the time adjustment may be accomplished by changing the number of the shift stages (i.e., a second latency setting) (e.g., col. 28, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to register a signal representing the data mask signal in response to a second clock edge of the clock signal for a second latency setting by changing the number of the shift stages (i.e., second latency setting) because it would allow time adjustment of inhibiting data output and increase system flexibility and performance as taught by Parks, (e.g., col. 28, lines 20-25; col. 3, lines 1-5).

As per claims 89 and 91, Park shows a method of selectively masking complimentary read data signals responsive to a data mask signal (e.g., figs. 26, 31-32, 54), comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and a second clock edge of the clock signal (e.g., col. 28, lines 1-25);

generating first and second coded read data signals corresponding to the complimentary read data signals, respectively, in the absence of the data mask signal

(e.g., figs. 26, DO, complementary DO, 288, 290, outputs from 294, 298; col. 37, line 35 to col. 38 line 20);

coding the first and second coded read data signals in a predetermined manner responsive to the data mask signal (e.g., figs. 26, 53, DO, complementary DO, els. 288, 290, outputs from els. 294, 298; col. 37, line 35 to col. 38 line 20);

Coupling a data output terminal to a first voltage node responsive to one of the data read output signals having a first predetermined logic level (e.g., figs. 26, 54, el. 308, DQ, els. Vcc, Vss, Vpp; col. 37, line 35 to col. 38 line 20);

Coupling the data output terminal to a second voltage node responsive to the other of the data read output signals having a second predetermined logic level (e.g., figs. 26, 54, el. 308, DQ, els. Vcc, Vss, Vpp; col. 37, line 35 to col. 38 line 20); and

Electrically isolating the data output terminal from the first and second voltage nodes if the coded read data signals are coded in the predetermined manner (e.g., figs. 26, 54, el. 308, DQ; col. 37, line 35 to col. 38, line 20). Parks does not explicitly shows a second latency setting; however, Parks teaches the time adjustment may be accomplished by changing the number of the shift stages (i.e., a second latency setting) (e.g., col. 28, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to register a signal representing the data mask signal in response to a second clock edge of the clock signal for a second latency setting by changing the number of the shift stages (i.e., second latency setting) because it would allow time adjustment of inhibiting data output and increase system flexibility and performance as taught by Parks, (e.g., col. 28, lines 20-25; col. 3, lines 1-5).

As per claims 80-82 and 86-88, Park shows the respective predetermined signals applied to the first and second output terminals of the first stage are any signals that are not complimentary to each other (e.g., fig. 26, outputs from els. 294, 298; col. 37, line 35 to col. 38 line 20); the predetermined signals correspond to logic “1” (e.g., fig. 26, outputs from els. 294, 298; col. 37, line 35 to col. 38 line 20); and the coupling of the first and second input terminals to the respective first and second output terminals of the first stage is delayed in time so that the complimentary first and second data signals are stored in the first stage for a predetermined time (e.g., figs. 26, els. 286, 286', 292; col. 37, line 35 to col. 38 line 20).

As per claims 84, 90 and 92, Park shows the predetermined manner of coding is for the coded read data signals to have the same value (e.g., fig. 26, outputs from els. 294,.298; col. 37, line 35 to col. 38 line 20)

11. Applicant's arguments filed 2/13/06 with respect to claims 54-57 and 60-69 of the divisional application 10/460,813 have been fully considered but they are not persuasive.

12. In the remarks, the applicant argued that neither the phiDQMF or phiDQM signals are generated in response to different clock edges according to the latency.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., different clock edge) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Parks teaches what in the claim are, registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and a second clock edge of the clock signal (e.g., col. 28, lines 1-25); Parks does not explicitly shows a second latency setting; however, Parks teaches the time adjustment may be accomplished by changing the number of the shift stages (i.e., a second latency setting) (e.g., col. 28, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to register a signal representing the data mask signal in response to a second clock edge of the clock signal for a second latency setting by changing the number of the shift stages (i.e., second latency setting) because it would allow time adjustment of inhibiting data output and increase system flexibility and performance as taught by Parks, (e.g., col. 28, lines 20-25; col. 3, lines 1-5).

In addition, Parks, col. 28, lines 5-25 and fig. 32, shows a mask signal DQM being generated in response to a high and low clock edges of CLK or phiCLK according to a first relay setting, a mask signal phiDQM being generated in response to a high and low clock edges of CLK or phiCLK a first relay setting, and phiDQMF being generated in response to a high and low clock edges of CLK or phiCLK a first relay setting.

13. Claims 4-6, 12-14, 20-22, 27-29, 35-37, 44-46, and 51-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and an alternate Friday and an alternate Monday, Thursday, and an alternate Friday from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-83007467-239 for Official communications, (703) 746-7240 for Non Official communications, and (571) 273-8300 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

D.T.
11/8/07